

first and second I/O slots arranged on the same wiring level in parallel along a peripheral portion of a chip within an inner region of the chip;

a first pad arranged on a wiring level different from said first I/O slot and arranged above the first I/O slot without being connected to the first I/O slot;

a second pad arranged on a wiring level different from said first I/O slot and arranged apart from the peripheral portion of the chip as compared with the first pad;

a first wiring comprising one end positioned in said first pad and comprising the other end positioned in the peripheral portion of the inner region of the chip above the first I/O slot;

looks like peripheral area

a second wiring comprising one end positioned in the second pad and comprising the other end positioned in the peripheral portion of the inner region of the chip above the second I/O slot; and

a third wiring arranged in an outermost peripheral region of the chip and serving to connect the other end of the first wiring to an I/O slot different from the first I/O slot.

REMARKS

By this Amendment, Applicants propose amending claim 1 to more clearly define the present invention. Thus, claims 1, 6-8, 10 and 15-20 will remain pending upon entry of this Amendment.

In the last Office Action, the Examiner rejected claims 1, 6-8, 10 and 15-20 under 35 U.S.C. § 112, second paragraph; and rejected claims 1, 6-8, 10 and 15-20 under 35 U.S.C. § 103(a) as unpatentable over Applicants' so-called admitted prior art (Fig. 4) in view of U.S. Patent No. 5,679,967 to Janai et al. ("Janai").

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